AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of making a semiconductor structure, comprising:

measuring a pattern density of a layer; followed by

calculating a first polish time, sufficient to planarize the layer on a semiconductor substrate;

polishing the layer for said first polish time, to planarize the layer; and

polishing the layer to a predetermined thickness.

2. (Previously Presented) The method of claim 1, further comprising, prior to the calculating of said first polish time, measuring the thickness of the layer.

3. (Canceled)

4. (Previously Presented) The method of claim 1, further comprising, prior to the calculating of said first polish time, identifying a composition of the layer.

5. (Original) The method of claim 1, further comprising determining a second polish time sufficient to reduce the thickness of the layer after planarization to the predetermined thickness;

wherein the polishing of the layer to the predetermined thickness comprises polishing the layer for said second polish time.

6. (Previously Presented) A process for making a plurality of semiconductor structures, comprising

making each semiconductor structure by the method of claim 1;

wherein a Cpk of the process is at least 1.

7. (Previously Presented) A process for making a plurality of semiconductor structures, comprising:

making each semiconductor structure by the method of claim 5;

wherein a Cpk of the process is at least 1.

8. (Previously Presented) The process of claim 7, wherein the making of each semiconductor structure comprises, prior to the calculating of said first polish time, measuring the thickness of the layer, a pattern density of the layer, and identifying a composition of the layer.

9-11. (Cancelled)

12. (Currently Amended) In a method of making a semiconductor structure, including polishing a layer by chemical mechanical polishing, the improvement comprising measuring a pattern density of the layer; followed by calculating a first polish time sufficient to make the layer planar; determining a second polish time to reduce the thickness of the planar layer; and polishing for a third polish time equal to the sum of the first and second polish times.

13. (Original) A method of making a semiconductor device, comprising:
making a semiconductor structure by the method of claim 1; and
forming a semiconductor device from said structure.

14. (Original) A method of making an electronic device, comprising:
making a semiconductor device by the method of claim 13; and
forming an electronic device, comprising said semiconductor device.

15. (Original) A method of making a semiconductor device, comprising:
making a semiconductor structure by the method of claim 5; and
forming a semiconductor device from said structure.

16. (Original) A method of making an electronic device, comprising:
making a semiconductor device by the method of claim 15; and
forming an electronic device, comprising said semiconductor device.

17-23. (Cancelled)

24. (Currently amended) A method of making a semiconductor structure, comprising:

measuring the pattern density of a layer on a semiconductor substrate ~~and~~ followed by polishing the layer with a system comprising:

a chemical mechanical polishing apparatus; and

machine readable medium, comprising code, imbedded in the machine readable medium, for calculating a first polish time, sufficient to planarize a layer on a semiconductor substrate.

25. (Original) A method of making a semiconductor device, comprising: making a semiconductor structure by the method of claim 24; and forming a semiconductor device from said structure.

26. (Original) A method of making an electronic device, comprising: making a semiconductor device by the method of claim 25; and forming an electronic device, comprising said semiconductor device.